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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIDMATIONING				
09/009,248	01/20/1998	KENJI OSAWA	P972636	CONFIRMATION NO.				
26263 7590 11/06/2002 SONNENSCHEIN NATH & ROSENTHAL								
P.O. BOX 061		EXAMINER						
WACKER DR CHICAGO, IL	IVE STATION 60606-1080	GRAYBILL, DAVID E						
			ART UNIT	PAPER NUMBER				
			2827	· · · · · · · · · · · · · · · · · · ·				
			DATE MAILED: 11/06/2002					

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No		Applicant(s)	
	•	09/009,248		OSAWA ET AL.	
Office Action Summary		Examiner		Art Unit	
		David E Graybi	ı	2827	
	- The MAILING DATE of this communication ap	pears on the cov	er sheet with the	correspondence ad	dress
Period fo	r Reply				
THE N - Exten after S - If the - If NO - Failur - Any re	DRTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. Is ions of time may be available under the provisions of 37 CFR 1. SIX (6) MONTHS from the mailing date of this communication. Period for reply specified above is less than thirty (30) days, a reperiod for reply is specified above, the maximum statutory period re to reply within the set or extended period for reply will, by statutely received by the Office later than three months after the mailing dispatent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, hor	wever, may a reply be ainimum of thirty (30) o e SIX (6) MONTHS fro to become ABANDO	timely filed lays will be considered timely om the mailing date of this co	/. mmunication.
1)⊠	Responsive to communication(s) filed on 08	March 2002 .			
2a)□	•	his action is non-	final.		
3)	Since this application is in condition for allow closed in accordance with the practice under	vance except for r <i>Ex par</i> te Quayl	formal matters, e, 1935 C.D. 11	prosecution as to th , 453 O.G. 213.	e merits is
-	on of Claims				
	Claim(s) 1-3 and 5-17 is/are pending in the a				
	4a) Of the above claim(s) 7-9 is/are withdrawr	n from considera	tion.		
5)	Claim(s) is/are allowed.				
6)⊠	Claim(s) <u>1-3,5,6 and 10-17</u> is/are rejected.				
	Claim(s) is/are objected to.				
	Claim(s) are subject to restriction and	or election requi	rement.		
	ion Papers				
	The specification is objected to by the Examin		b tha F		
10)	The drawing(s) filed on is/are: a) acc	cepted or b) obje	ected to by the	xammer.	
_	Applicant may not request that any objection to t	the drawing(s) be	neid in abeyance. wod b\□ disan	proved by the Evamin	ner
11)	The proposed drawing correction filed on			proved by the Examin	101.
40.	If approved, corrected drawings are required in r		action.		
•	The oath or declaration is objected to by the E	_xammer.			
	under 35 U.S.C. §§ 119 and 120	ian neigrity under	25110 (8.11	9(a)-(d) or (f)	
	Acknowledgment is made of a claim for forei	igh phonly under	33 0,3.0. 3 11	5(a) (a) 51 (i).	
a)	D□ All b)□ Some * c)□ None of:	ento hovo hoon re	ocaived		
	1. Certified copies of the priority docume			cation No	
	2. Certified copies of the priority docume				l Stane
*	 Copies of the certified copies of the pr application from the International E See the attached detailed Office action for a li 	Bureau (PCT Ru	e 17.∠(a)).		. Otago
	Acknowledgment is made of a claim for dome				al application).
	a) ☐ The translation of the foreign language p Acknowledgment is made of a claim for dome	provisional applic	ation has been	received.	
Attachme		•			
1) Not	ine of References Cited (PTO-892) ice of Draftsperson's Patent Drawing Review (PTO-948) ormation Disclosure Statement(s) (PTO-1449) Paper No(s	•	Interview Sum Notice of Infor Other:	mary (PTO-413) Paper N mal Patent Application (F	lo(s) PTO-152)

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The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 5, 6, 10, 12-14, 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly the subject matter which applicant regards as the invention.

In claims 1 and 5 the limitation "the sealing ring" is unclear because the limitation refers to a "sealing ring" but there is no apparent previous claim-recitation of a sealing ring.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a),

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the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5, 6 and 10-12 are rejected under 35 U.S.C. 103(a) as obvious over the combination of Ohsawa (5756377) and Yamasaki (5554885).

At column 4, lines 25-29, column 5, lines 8-11, column 6, lines 53-56, column 7, line 67 to column 8, line 7, and column 9, line 18 to column 10, line 17 Ohsawa teaches the following:

1. A semiconductor device, comprising: a semiconductor chip
4 having a plurality of electrode pads formed at a periphery of
a front surface thereof; a wiring film formed on a front surface
side of said semiconductor chip by laminating an insulation film
6 on a lead 13 pattern; an outer connection terminal 7 formed so
as to protrude above said wiring film; a plurality of leads 13
extending from said wiring film and connected to the electrode
pads on said semiconductor chip at extended tip ends 13i

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thereof; an external ring 10 provided so as to surround said semiconductor chip and formed with a plurality of holes positioned entirely outside of a perimeter edge of the semiconductor chip; and a sealing resin 8 filled between said semiconductor chip and said external ring the sealing resin further being filled in the through holes to increase the contact between the sealing resin and the external ring which strengthens the bond between the sealing ring and the external ring.

- 2. A semiconductor device according to 1, further comprising an outwardly expanded open portion formed on an inner circumferential surface of said external ring and positioned on a rear surface side of said semiconductor chip.
- 3. A lead frame, comprising: a wiring film formed by laminating an insulation film 6 on a lead 13 pattern; an external connection terminal 7 formed so as to protrude above said wiring film; a plurality of leads 13 extending from said wiring film and forming connecting portions to electrode pads on a semiconductor chip 4 at extended tip ends 13i thereof; and an external ring 10 provided outside said wiring film, having an opening portion capable of housing said semiconductor chip and formed with a plurality of holes positioned entirely outside of a perimeter edge of the semiconductor chip when the opening

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portion houses the semiconductor chip wherein an outwardly extending open portion is formed on the opening portion and positioned on a rear surface side of the semiconductor chip.

5. An electronic apparatus including a printed wiring board loaded with a semiconductor chip, said semiconductor device, comprising: a semiconductor chip 4 having a plurality of electrode pads formed at a periphery of a front surface thereof; a wiring film formed on a front surface side of said semiconductor chip by laminating an insulation film 6 on lead 13 patterns; an outer connection terminal 7 formed so as to protrude above said wiring film; a plurality of leads 13 extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tip ends 13i thereof; an external ring 10 provided so as to surround said semiconductor chip and, formed with a plurality of holes positioned entirely outside of a perimeter edge of the semiconductor chip; and a sealing resin 8 filled between said semiconductor chip and said external ring, the sealing resin further being filled in the through holes to increase the contact area between the sealing resin and the external ring which strengthens the bond between the sealing ring and the external ring, wherein said external connection terminal and an electrode on said printed wiring board are connected.

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6. An electronic apparatus according to 5, further
comprising an outwardly expanded open portion formed on an inner
circumferential surface of said external ring and positioned on
a rear surface side of said semiconductor chip.

10. A semiconductor device according to 1, wherein the
external ring has an open top and an open bottom and is entirely

11. A lead frame device according to 3, wherein the external ring has an open top and an open bottom and is entirely spaced away from the semiconductor chip when the opening portion

spaced away from the semiconductor chip.

houses the semiconductor chip.

12. An electronic apparatus according to 5, wherein the external ring has an open top and an open bottom and is entirely spaced away from the semiconductor chip.

Although, as cited, Ohsawa teaches all of the limitations of the instant invention, including a device and an apparatus formed with a plurality of holes positioned entirely outside of a perimeter edge of the semiconductor chip, and a device comprising wherein the external connection terminal and an electrode on a printed wiring board are connected, these limitations do not appear to be explicitly taught in one embodiment containing all of the instant limitations.

Nonetheless, it would have been obvious to combine these

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particular limitations of the embodiments of Ohsawa because it would facilitate miniaturization, manufacturing convenience and external electrical connection.

To further clarify the teachings of an outwardly expanded open portion formed on an inner circumferential surface of said external ring and positioned on a rear surface side of said semiconductor chip, and wherein an outwardly extending open portion is formed on the opening portion and positioned on a rear surface side of the semiconductor chip, attention is directed to Figure 6B, wherein these limitations are illustrated.

However, Ohsawa does not appear to explicitly teach the sealing resin further being filled in through holes to increase the contact between the sealing resin and the external ring which strengthens the bond between the sealing ring and the external ring.

Notwithstanding, at column 6, lines 5-12, column 6, line 28 to column 7, line 4, and column 9, line 62 to column 10, line 56, Yamasaki teaches a sealing resin 50, 52 further being filled in through holes 14, 16 to increase the contact between the sealing resin and an external ring 10 which strengthens the bond between the sealing resin and the external ring. Moreover, it would have been obvious to combine the product of Yamasaki with

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the product of Ohsawa because it would strengthen the bond between the sealing resin and the external ring.

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ohsawa and Yamasaki as applied to claims 1-3, 5, 6 and 10-12, and further in combination with Hassan (5773895).

The combination of Ohsawa and Yamasaki does not appear to explicitly teach wherein the sealing resin is filled in blind holes in the external ring.

Regardless, at column 3, lines 1-15, Hassan teaches that blind holes are functional equivalents in a product wherein sealing resin is filled in a package substrate, similar to the product of the combination of Ohsawa and Yamasaki. Furthermore, it would have been obvious to combine the product Hassan with the product of the combination of Ohsawa and Yamasaki because it would strengthen the bond between the sealing resin and the external ring.

Applicant's remarks filed 3-8-2 have been fully considered and are adequately addressed in the rejection supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

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Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill Primary Examiner Art Unit 2827

D.G. 30-Oct-02